|  |  |
| --- | --- |
| Faculty of Computer & Information Sciences  Ain Shams University  Subject: CHW-362Computer Architecture & Org.  Instructors: Dr. Heba Khaled & Dr. Karim Emara  Year: 3rd year undergraduate  Academic year: 2nd term 2019-2020 |  |

**Practical Project**

**MIPS Pipelined Emulator – Version ( 2)**

**تحذير هام: علي الطالب عدم كتابة اسمه أو كتابة اي شيء يدل علي شخصيته**

**Task 1:**

Fill the Table as per the questions sheet description

Table 1 MIPS Machine Code

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **MIPS Code** | **Type** | **Machine Code** | | | | | | | |
| **opcode** | **rs** | **rt** | | **rd** | | **shamt** | **funct** |
|  |  | |  | | ***Address/Immediate*** | | |
| **1000: or $5, $6, $Zero** | **R** | **0** | **6** | **0** | | **5** | | **0** | **37** |
| **1004: add $2, $3, $4** | **R** | **0** | **3** | **4** | | **2** | | **0** | **32** |
| **1008: sub $7, $8, $6** | **R** | **0** | **8** | **6** | | **7** | | **0** | **34** |
| **1012: sw $5, 2($30)** | **I** | **43** | **30** | **5** | |  | | **2** |  |
| **1016: and $6, $5, $Zero** | **R** | **0** | **5** | **0** | | **6** | | **0** | **36** |
| **1000: or $5, $6, $Zero** | **R** | **0** | **6** | **0** | | **5** | | **0** | **37** |

Table 2 MIPS Pipelined Data-Path values for 9 Clock Cycles

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Data input/output | | CC1 | CC2 | CC3 | CC4 | CC5 | CC6 | CC7 | CC8 | CC9 |
| [1] PC | | 1000 | 1004 | 1008 | 1012 | 1014 |  |  |  |  |
| [2] Adder1output | | 1004 | 1008 | 1012 | 1014 | 1016 |  |  |  |  |
| Register File | [3] Read Register 1 |  | 6 | 3 | 8 | 30 | 5 |  |  |  |
| [4] Read Register 2 |  | 0 | 4 | 6 | 5 | 0 |  |  |  |
| [5] Read Data 1 |  | 106 | 103 | 108 | 130 | 150 |  |  |  |
| [6] Read Data 2 |  | 0 | 104 | 106 | 105 | 0 |  |  |  |
| [7] Write Register |  | 5 | 2 | 7 | -- | 6 |  |  |  |
| [8] Write Data |  | ??? | ??? | ??? | ??? | ??? |  |  |  |
| [9] Inst [15-0] | |  | 10277 | 4128 | 14370 | 2 | 12324 |  |  |  |
| [10] Inst [16-20] | |  | 0 | 4 | 6 | 5 | 0 |  |  |  |
| [11] Inst [15-11] | |  | 5 | 2 | 7 | -- | 6 |  |  |  |
| ALU | [12] ALU\_Input 1 |  |  | 106 | 103 | 108 | 130 | 150 |  |  |
| [13] ALU\_MUX I/P 0 |  |  | 0 | 104 | 106 | 105 | 0 |  |  |
| [14] ALU\_MUX I/P 1 |  |  | X | X | X | 2 | X |  |  |
| [15] ALU\_MUX O/P |  |  | 0 | 104 | 106 | 2 | 0 |  |  |
| [16] ALU O/P |  |  | 106 | 207 | 2 | 132 | 0 |  |  |
| [17] rt\_RegDst\_Mux I/P 0 | |  |  | 0 | 4 | 6 | 5 | 0 |  |  |
| [18] rdRegDst\_Mux I/P 1 | |  |  | 5 | 2 | 7 | -- | 6 |  |  |
| [19] regDist\_MUX O/P | |  |  | 5 | 2 | 7 | X | 6 |  |  |
| [20] Adder2 Input 1 | |  |  | X | X | X | X | X |  |  |
| [21] Adder2 Output | |  |  | X | X | X | X | X |  |  |
| [22] Ex/Mem Add Output | |  |  |  | X | X | X | X | X |  |
| Data Memory | [23] Address |  |  |  | 106 | 207 | 2 | 132 | 0 |  |
| [24] Write Data |  |  |  | 0 | 104 | 106 | 105 | 0 |  |
| [25] Read Data |  |  |  | ! | ! | ! | ! | ! |  |
| [26] EX/MEM.RegisterRd | |  |  |  | 5 | 2 | 7 | X | 6 |  |
| [27] MemToReg\_Mux I/P 1 | |  |  |  |  | ! | ! | ! | ! | ! |
| [28] MemToReg\_Mux I/P 0 | |  |  |  |  | 106 | 207 | 2 | 132 | 0 |
| [29] MemToReg\_Mux O/P | |  |  |  |  | 106 | 207 | 2 | X | 0 |
| [30] MEM/WB.RegisterRd | |  |  |  |  | 5 | 2 | 7 | X | 6 |

X: do not care

!: can not access

???: not calculated yet

[20] to [22] do not care in this version

Table 3 MIPS Pipelined ControlSignal for 9 Clock Cycles

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Control Signal | CC1 | CC2 | CC3 | CC4 | CC5 | CC6 | CC7 | CC8 | CC9 |
| PCSrc | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| RegWrite |  |  |  |  | 1 | 1 | 1 | 0 | 1 |
| ALUop (2 bits) |  |  | 10 | 10 | 10 | 00 | 10 |  |  |
| ALUSrc |  |  | 0 | 0 | 0 | 1 | 0 |  |  |
| RegDst |  |  | 1 | 1 | 1 | X | 1 |  |  |
| MemWrite |  |  |  | 0 | 0 | 0 | 1 | 0 |  |
| MemRead |  |  |  | 0 | 0 | 0 | 0 | 0 |  |
| MemtoReg |  |  |  | 0 | 0 | 0 | 0 | X | 0 |

# **LMS Submission guidelines**

* Take care to submit your research not at the last minute, so as to meet the submission successfully without any tension.
* Be sure your submissions are the correct files you mean to submit, because once the submission is done, you cannot undo the operation or resubmit again.
* Do not name your submitted files with your name or ID.
* PDF file for Task 1 Report. File name must be of the following format: V1\_Task1.**pdf**

(V1 is for version1, use your exam version number after the letter V.)